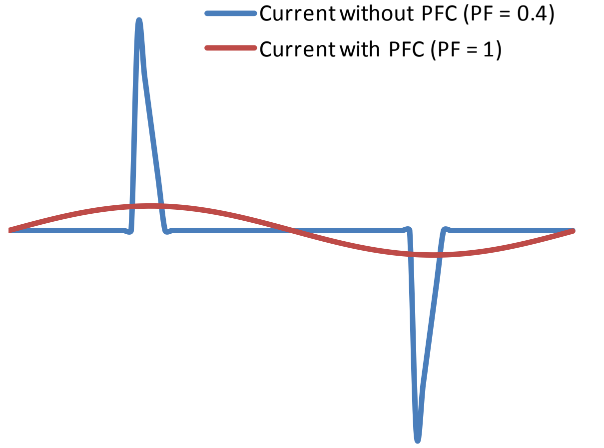
Power Factor Correction: An Energy Efficiency Perspective

Power factor (PF) is an often misunderstood metric that represents the ratio of "real" ac power consumed by an electrical load[1] to the amount of "apparent" power that needs to travel on the grid (a simple product of the average current times the average voltage, which dictates the size of conductors and power losses in transformers and distribution). An ideal device has a PF of 1, where a product draws the same amount of apparent power as real power, which means the current waveform is a pure sine wave that is in perfect sync with the ac voltage of the grid. Unfortunately, most devices we use today do not behave this way. Mechanical loads like motors still draw current as sine waves, but these are slightly out of sync with the voltage. This creates a PF less than 1.[2] Electronics typically use switch mode power supplies (SMPS) that draw current in short spikes which often bear no relation to the voltage waveform, resulting in a PF as low as 0.4 if uncorrected.

Why does low PF matter to the energy efficiency community? Devices with low PF have proportionately higher ac current draw, which increases the resistive or I^2R losses in the building wiring. An electronic device with a PF of 0.4 draws 2.5 times the current compared to an ideal load with a PF of 1. Building wiring losses could be 6.25 times higher than the ideal case! Though the current drawn by an individual device is relatively small, all of the electronic devices draw the current spike at the same time, so the total current and thus loss can be significant.

Electric utilities typically encourage higher power factor through their commercial and industrial rate structures – mostly to maximize the power carrying capacity of transmission and distribution lines and to improve system reliability.[3] However, very little effort has been made to address PF in smaller devices like electronics, which are the focus of this report. The EU currently regulates PF for loads greater than 75 W. The ENERGY



Current draw over one 60 Hz cycle for a 100 W device with and without PFC.

STAR version 5.0 specification for computers requires that desktop computer power supplies have a PF greater than 0.9 at the full rated load. In California, TVs greater than 100 W in load require power factor correction (PFC). Overall, very little global effort has been made to address power factor from the standpoint of energy efficiency.

PFC Techniques

The simplest technique to increase PF in SMPS is resizing existing components to improve congruence between the current and voltage waveforms (e.g. reducing the capacitor size to increase the current conduction time). This PFC approach can raise PF to about 0.6 and can cut the building wiring losses associated with the load in half. However, the dc voltage provided to the device by the SMPS fluctuates significantly, which is only acceptable for a limited number of dedicated battery charger products, like cordless power tools. This severely limits the application and potential energy savings for this technology.

So-called "passive" and "active" PFC techniques directly control the shape of the current waveform, further boosting PF. Passive PFC involves the use of additional analog control components (such as inductors and capacitors) and can achieve PF as high as 0.8; however, the cost and power required for these circuits generally prohibits their use. The use of "active" digital controllers in PFC is the current state of the art, having higher efficiency and lower cost than passive PFC. The first digital active PFC patent was issued in 1987, and manufacturers like ON Semiconductor and Power Integrations now offer effective, low-power, inexpensive integrated circuits capable of achieving PF of

[1] The integration of current and voltage over a complete cycle of the ac waveform – it represents real work.

[2] By convention, a "lagging" or inductive load, such as a motor, has positive reactive power. A "leading", or capacitive load, such as a microwave oven, has negative reactive power.

[3] Utilities are also concerned about current harmonics, which are caused by SMPS that are not PF corrected. When multiple SMPS devices are present in a three phase wiring system, such as those used in most commercial buildings, they can sum together and exceed the current rating of the neutral line, causing it to overheat.

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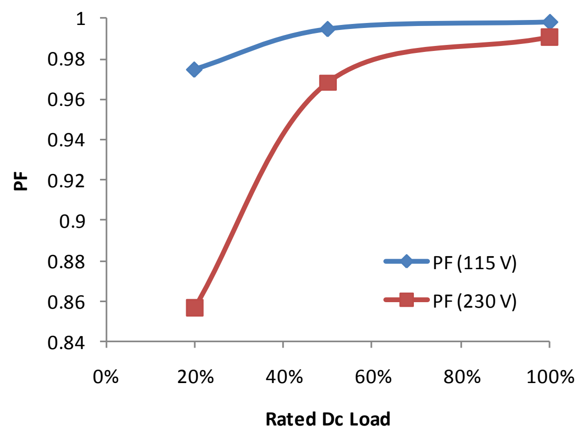
up to 0.99, although 0.9 is a typical figure. The latest products consume little additional power, incurring a 1 to 1.5% penalty on the SMPS's overall ac-dc conversion efficiency. Cost is fairly independent of the power of the device, so digital active PFC is more cost-effective for larger devices such as desktop computers.

State-of-the-Art PFC Technology

Below is an image of a 300 W, dual-output SMPS (+12Vdc main output, +5Vdc standby output) that Ecos tested as part of the 'Ac-Dc Power Supplies' report. The SMPS is comprised of an ON Semiconductor PFC front end driving a Power Integrations SMPS back end.

ON Semiconductor PFC (left) and Power Integrations switch mode PS (right).

Ecos tested this unit, and found that the PFC circuit had an effective 95% efficiency, compared to 96% for a typical SMPS front end.[4] As shown at right, the PF falls slightly at part load, but remains over 0.9 for most operating conditions. This is an important feature to achieve high operational PF in electronics products, because most electronics only place a partial load on their power supply the majority of the time.



Power Factor Under Varying Load Conditions

The Savings Factor

Energy savings achieved by lowering building wiring losses are difficult to estimate because there are uncertainties in the average loading of branch circuits, the load profile, branch circuit length, wiring configuration, wire thickness, and the PF of the other loads on the system. Regardless, order-of-magnitude estimates are possible that indicate the size of the opportunity. In the table below, savings are estimated for digital active PFC (PF = 0.9). The net savings is the savings in building wiring minus the efficiency penalty incurred by adding active PFC circuitry. The residential assumption is that all the electronic loads are on three circuits; commercial is six 90 W computer/monitor systems per circuit. The upstream multiplier is the ratio of total energy savings (including wiring losses up to the distribution transformer) to energy savings on the circuit. The wiring savings for commercial are 3.5 times as large as residential because of the longer circuit and higher usage (despite thicker wire and lower upstream multiplier), but the net savings are 5 times as large.

Large energy-using residential electronics are likely to be cost-effective for active PFC, such as personal electric vehicles (bicycles, wheelchairs, etc.), TVs, desktop computers, and some set-top boxes. Since the energy savings in a commercial setting is a higher percentage, active PFC in the medium energy using electronics (laptops) as well as the large energy using electronics (linear fluorescent lamps, desktops, and computer monitors) should be cost-effective as well. The global energy savings potential would be roughly 3 TWh per year,[5] or the equivalent of taking one typical coal-fired power plant out of operation.

[4] SMPS commonly have a preregulator used to accept the wide range of ac input voltages found around the world and to better accommodate power fluctuations.

[5] Total PS energy use in 2006 is ~600,000 GWh per year. With 7% growth per year, this would be 860,000 GWh per year in 2011. We assume that PFC applies to 10% of this load and achieves 4% average reduction in losses (more residential devices than commercial).

Savings Due to PFC

Scenario	Residential	Commercial
kWh/yr/circuit	400	1200
Hr/day high use	6.0	6.0
Circuit length (one way, m)	12	30
Wire thickness	14 AWG ($2.1\ mm^2$)	12 AWG ($3.3\ mm^2$)
Resistance (ohms)	0.20	0.31
PF all loads initially	0.40	0.40
RMS current during high use (A)	3.0	8.9
I^2R circuit loss during high use (W)	1.8	25
I^2R circuit loss during high use if all PF = 1 (W)	0.29	3.9
Upstream multiplier	2.0[6]	1.5[7]
Wiring savings (of marginal device energy)[8]	3.3%	12%
Net savings (of device energy)	2.1%	11%

Next Steps

The economics of PFC technology will change over time. As more devices have PFC, the savings from adding PFC to an additional device falls because of the I^2R behavior. However, total energy use of electronics has been rising sharply, while the number of circuits has not risen very fast. This would tend to increase the savings from PFC. Furthermore, as the technology improves, the incremental cost and efficiency penalty should fall. Therefore, PFC should become cost-effective in smaller and smaller devices over time.

Some utilities have PF requirements for large customers to reduce transmission and distribution energy losses. Building or grid-level PFC can be used to address these problems, but the disadvantage is that energy is not saved on the branch circuits to individual devices, which is where the majority of the total energy savings is possible. The advantage of building or grid-level PFC is that it would apply to all loads.

It should be pointed out that simply increasing the energy efficiency of devices with the same power factor reduces wiring losses as well, but in devices where further power supply efficiency improvements are no longer feasible, PFC could be a cost-effective alternative.

An alternative way of reducing energy loss in building wiring is to use lower resistance wires. Using aluminum wires of the alloy types that have been shown not to cause fires would be a particularly cost-effective way of doing this. This could save approximately 1% of all electricity cost-effectively, or 200 TWh per year, a much larger impact than PFC because the wires apply to all electric devices, not just large power supplies.

More research into quantifying the building wiring energy loss in the field for both residential and commercial would be very beneficial because of the large uncertainties currently.

[6] Estimate – should be larger than commercial because the circuit loss for residential is smaller.
[7] "Assessment of the Impacts of Power Factor Correction in Computer Power Supplies on Commercial Building Line Losses," Brian Fortenbery and Jonathan G. Koomey, Ph.D. Prepared for the California Energy Commission, March 31, 2006
[8] Assuming that electronics use 75% of total energy in active mode. The marginal savings is double the average savings because of the I^2R behavior.